700V 140mΩ SolidGaN with Si MOSFET Compatibility

1. Features

- 140mΩ E-Mode GaN with Built-In Gate Clamp
- 700V Continuous, 750V Pulsed Voltage Rating
- Wide 8V to 20V Gate Input Voltage Range
- Adjustable Turn-On and Turn-Off Slew Rate
- Drop-In Replacement for Si MOSFET
- Work with Si MOSFET Controllers and Drivers
- Zero Reverse Recovery Charge
- Short Circuit Protection with Built-In DESAT
- Available in TO220 FullPAK Package

2. Applications

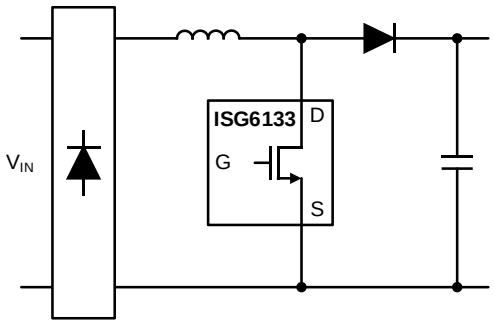
- Boost PFC, QR Flyback Topology
- AHB, LLC Topology
- AC-DC Power Adaptor, LED Lighting
- TV Power, Home Appliance Power

3. Description

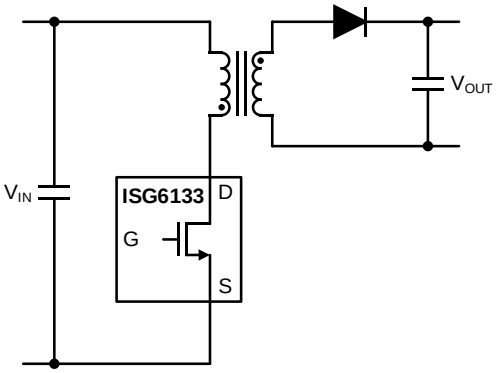
The ISG6133 SolidGaN IC seamlessly integrates a 700V enhanced mode Gallium Nitride (GaN) FET with a built-in gate clamp and DESAT protection in a conventional TO220 FullPAK package, establishing a new standard for performance, ease of use, and reliability in power electronics. It provides self-powered features without requiring a sustainable supply voltage for internal supply, ensuring consistent driving of integrated GaN FET. With built-in DESAT protection, the ISG6133 further ensures device robustness and system safety.

The ISG6133 offers the ability to adjust the turn-on slew rate of the GaN FET using an external gate resistor, allowing users to optimize efficiency and EMI performance. The ISG6133's high integration level with a GaN FET and robust protection makes it suitable for wide range of Si MOSFET applications with simple drop-in replacement.

4. Typical Application



< Boost PFC>



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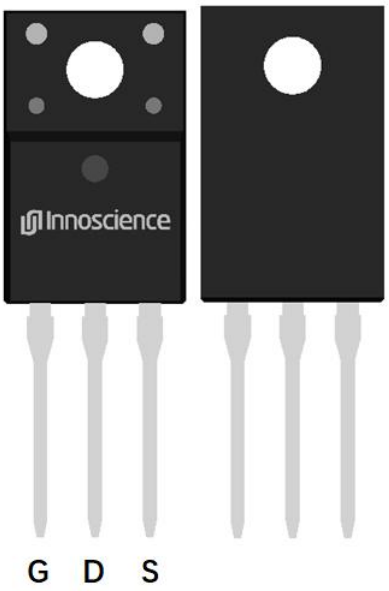
5. Revision History

Major changes since the last revision

Revision	Date	Description of Changes
1.0	2025-03-28	Final datasheet release

6. Pin Configuration and Functions



3-Lead TO220 FullPAK Package – Top and Bottom View

Pin Number	Pin Name	Description
1	G	Gate Input. Connect to the drive output of controller or gate driver.
2	D	Drain of Power GaN FET.
3	S	Source of Power GaN FET.

7. Absolute Maximum Ratings

All pins are referred to S pin, unless otherwise specified. Stress beyond the absolute maximum ratings can cause permanent damage or deteriorate device lifetime.

Parameter	Value	Unit
Drain Voltage, Continuous	700	V
Drain Voltage, Pulsed (1)	750	V
Drain Current, Continuous (T_C = 25°C)	18	A
Drain Current, Pulsed (10us @ T_C = 25°C)	32	A
Drain Current, Pulsed (10us @ T_C = 125°C)	18	A
Gate Voltage, Continuous	-0.6 to 20	V
Gate Voltage, Pulsed (1)	-5 to 24	V
Power Dissipation	27.2	W
Operating Junction Temperature T_J	-40 to 150	˚C
Storage Temperature	-55 to 150	˚C

(1) Intended for repetitive events, t_{PULSE} <100ns.

8. ESD Ratings

T_J = 25°C unless otherwise specified.

Parameter	Value	Unit
Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002	±1000	V

9. Recommended Operating Conditions

Parameter	Min	Max	Unit
Gate Input High Voltage	8	20	V
Gate Input Low Voltage	-0.3	0.3	V
Operating Junction Temperature	-40	125	˚C

10. Thermal Information

Symbol	Parameter	ISG6133TJ	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	48.3	˚C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.6	˚C/W

According to standards defined in JESD51 and JESD51-1, thermal characteristics of the package are simulated. $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

11. Electrical Characteristics

T_J = 25°C, V_{GS} = 12V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Gate Characteristic						
Gate input threshold voltage	V_{GS_TH}	3.6	4	4.4	V	
Gate quiescent current	I_{GON_Q}		200		uA	V_{GS} = 12V
Protection						
DESAT protection threshold (2)	V_{DS_DESAT}		5.9		V	
DESAT blanking time (2)	t_{BLK_DESAT}		600		ns	
Power GaN FET						
Drain-source leakage current	I_{DSS}		0.6 7	25	uA uA	V_{GS}=0V, V_{DS}=700V, T_J=25°C V_{GS}=0V, V_{DS}=700V, T_J=150°C
Drain-source resistance	$R_{DS(ON)}$		106 230	140	mΩ	V_{GS}=12V, I_{DS}=5A; T_J=25°C V_{GS}=12V, I_{DS}=5A; T_J=150°C
Source-drain reverse voltage	V_{SD}		2.4		V	V_{GS}=0V, I_{SD}=5A
Total gate charge (2)	Q_G		3.5		nC	V_{GS}=0V, V_{DS}=0 to 400V
Output charge (2)	Q_{OSS}		33		nC	V_{GS}=0V, V_{DS}=0 to 400V
Reverse recovery charge (2)	Q_{RR}		0		nC	V_{DS}=400V, I_{SD}=5A
Input capacitance (2)	C_{ISS}		125		pF	V_{GS}=0V, V_{DS}=400V, f=100kHz
Output capacitance (2)	C_{OSS}		41		pF	V_{GS}=0V, V_{DS}=400V, f=100kHz
Effective output capacitance, energy related (2)	$C_{O(er)}$		59		pF	V_{GS}=0V, V_{DS}=0 to 400V
Effective output capacitance, time related (2)	$C_{O(tr)}$		82		pF	V_{GS}=0V, V_{DS}=0 to 400V

12. Switching Characteristics

T_J = 25°C, V_{GS} = 12V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Turn-on propagation delay	t_{ON_PD}		50		ns	
Turn-off propagation delay	t_{OFF_PD}		30		ns	

(2) Not 100% tested and guaranteed by design.

13. Typical Characteristics

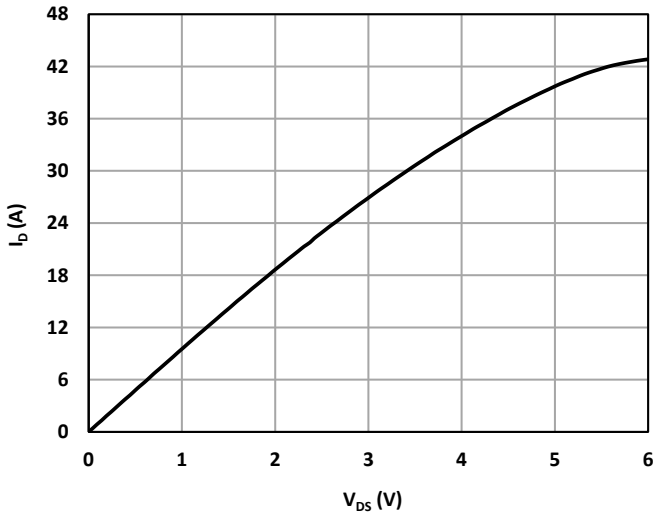


Figure 1. Drain Current vs Drain-to-Source Voltage, T_J=25°C

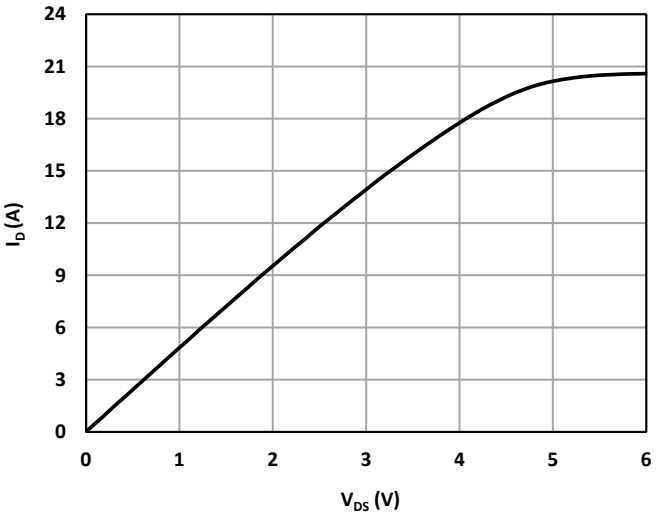


Figure 2. Drain Current vs Drain-to-Source Voltage, T_J=125°C

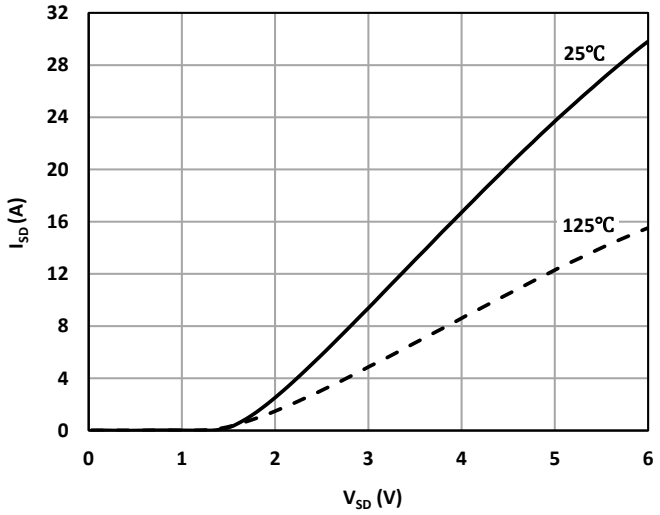


Figure 3. Source-Drain Reverse Conduction Current vs Voltage

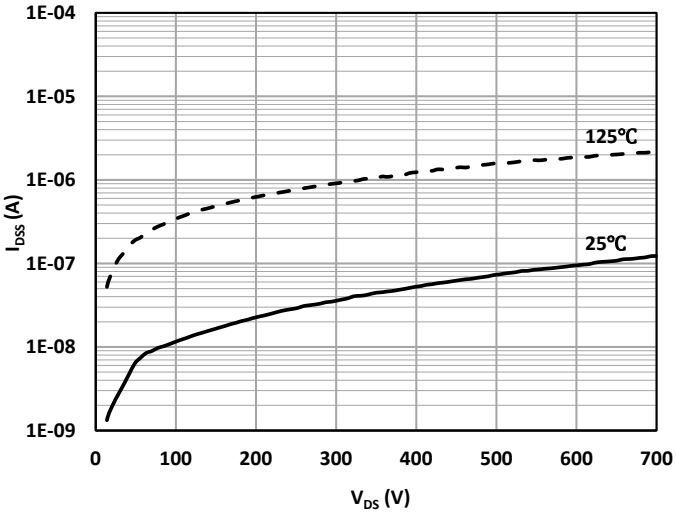


Figure 4. Drain Leakage Current vs Drain Voltage

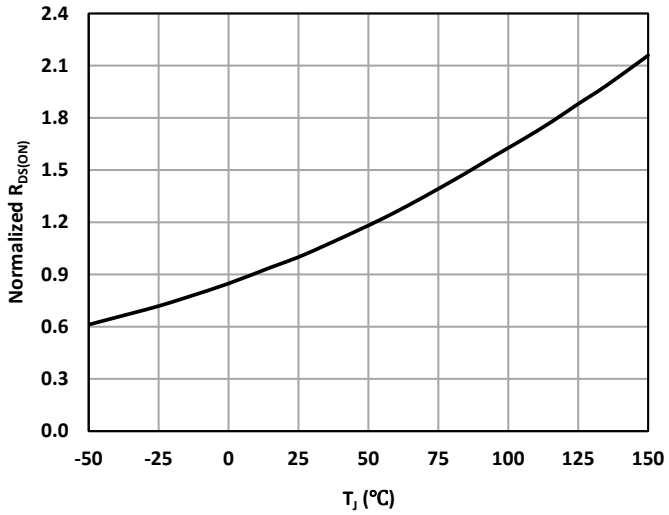


Figure 5. Normalized $R_{DS(ON)}$ vs Temperature

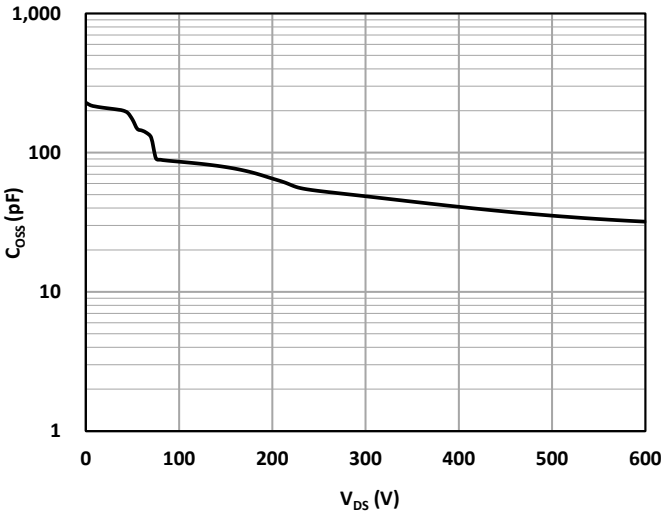


Figure 6. Output Capacitance vs Drain Voltage

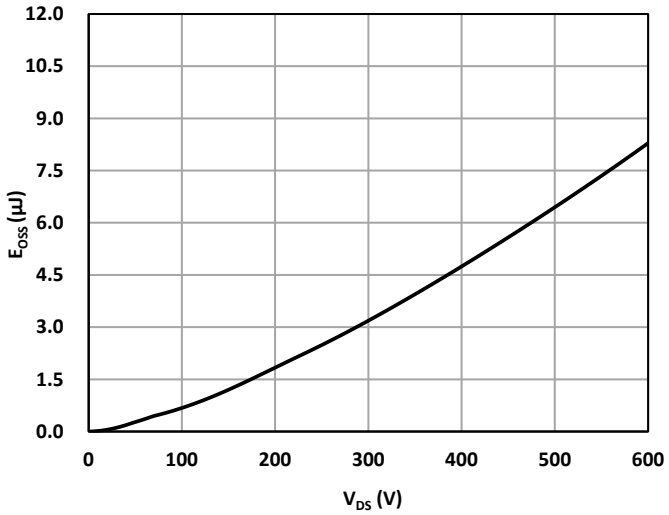


Figure 7. Output Capacitance Stored Energy vs Drain Voltage

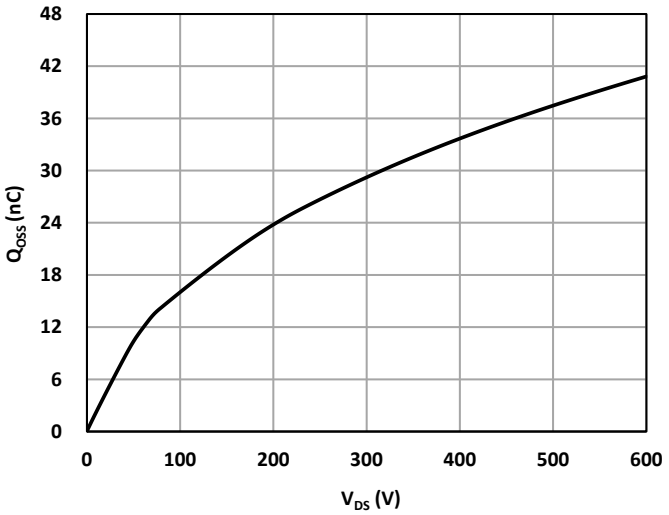


Figure 8. Output Charges vs Drain Voltage

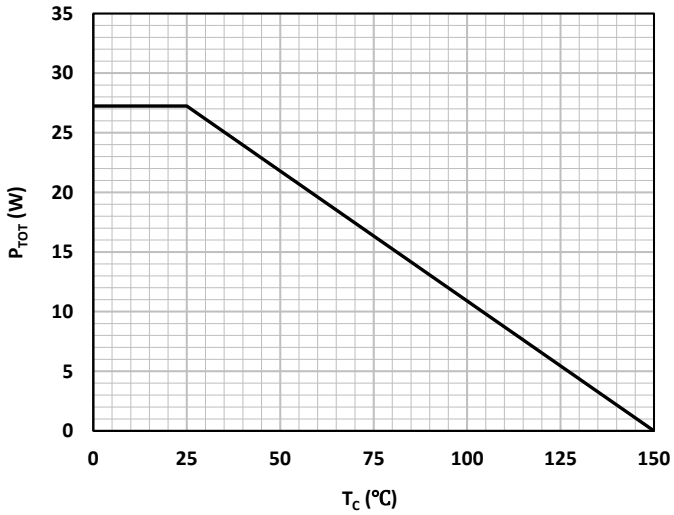


Figure 9. Power Dissipation

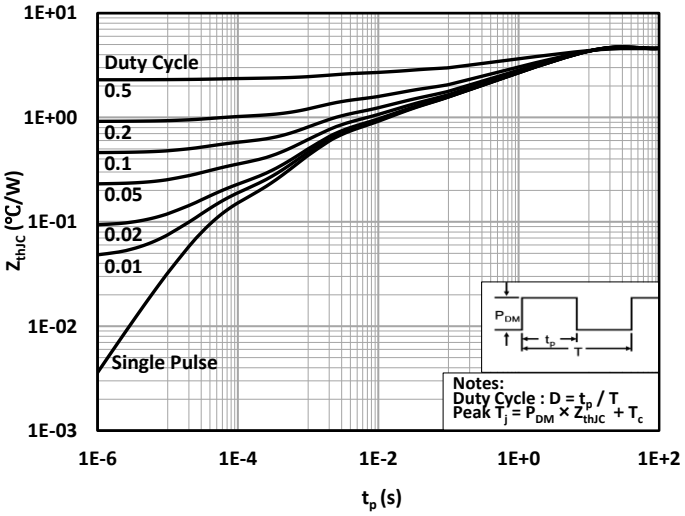


Figure 10. Max. Transient Thermal Impedance

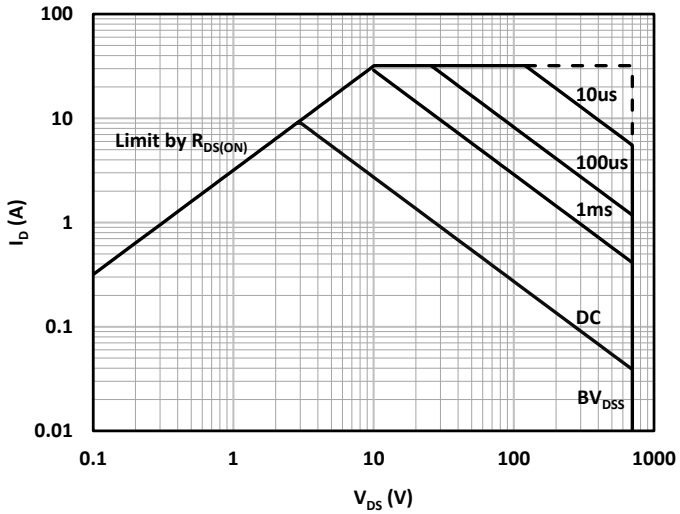


Figure 11. Safe Operating Area, T_J=25°C

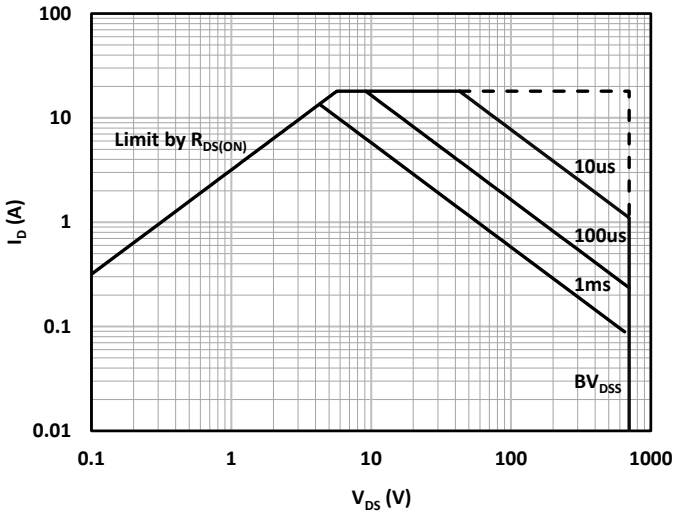


Figure 12. Safe Operating Area, T_J=125°C

14. Block Diagram

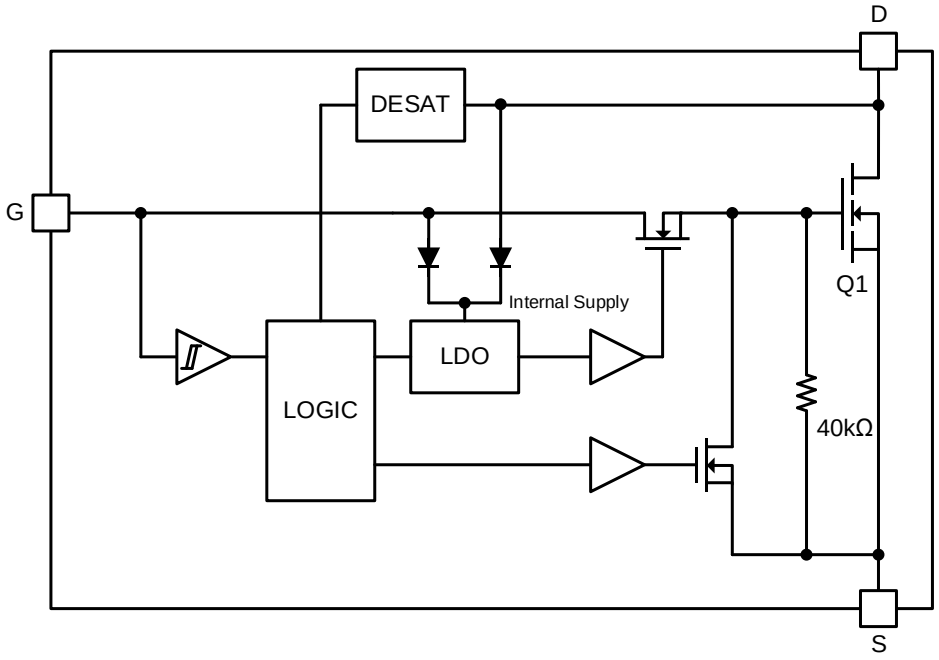


Figure 13. Functional Block Diagram

15. Function Description

The ISG6133 SolidGaN IC in a TO220 FullPAK package contains high performance E-mode GaN FET with a built-in gate clamp and DESAT protection. It incorporates a self-powered feature without specified supply voltage for internal circuitry, converting supply either G or D pin corresponding its operation. This ensures consistent driving of GaN FET with easy-of-use and reliable operation.

The ISG6133 enables the independent adjustment of turn-on slew rate for driver by an external gate resistor, optimizing both EMI performance and efficiency. With the high integration level of GaN FET and robust protection, the ISG6133 offers a simple setup with a low component count, ensuring it is suitable for high-frequency and high-power applications.

Power-On-Sequence and Self-Powered Operation

The ISG6133 offers the self-powered feature without sustainable supply voltage for internal supply (VDD). It converts supply either G or D pin according to operation states to guarantee consistent driving of GaN FET.

Figure 14 shows the switching characteristics of the G and D. When the system is powered on, D pin is pulled high, the internal supply is powered from the D pin. The D voltage exceeding 30V is required for proper power supply typically. When G pin voltage goes above 4.0V, the internal GaN FET turns on with a time delay, t_{ON_PD}, and the D is pulled down to ground, powering the internal supply from G pin. When the G pin voltage goes below 4.0V, the internal GaN FET turns off with a time delay, t_{OFF_PD}.

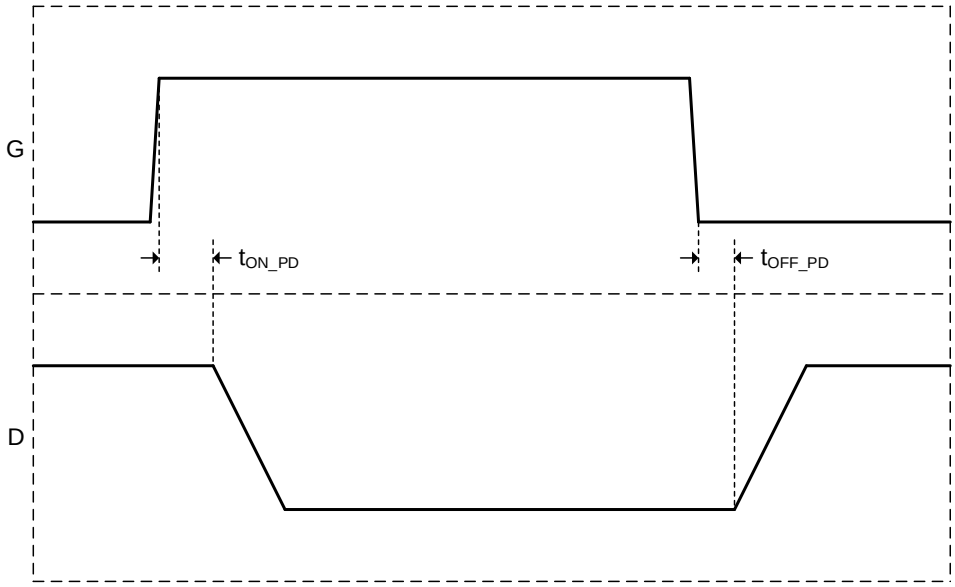


Figure 14. Timing Diagram of Input and Output

Adjustable Turn-On and Turn-Off Slew Rate

The ISG6133 supports users the ability to adjust both turn-on and turn-off slew rate of the GaN FET independently. This is achieved by adding external gate resistors and diode between the driver output and G pin of ISG6133 as shown in Figure 15, targeting optimization of efficiency, reliability, and EMI performance.

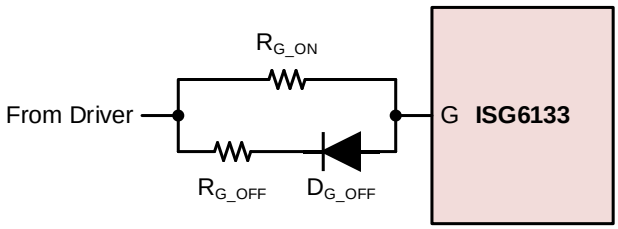


Figure 15. Configuration of Adjustable Turn-On Slew Rate

DESAT Protection

The ISG6133 provides cycle-by-cycle DESAT protection by monitoring the drain-source voltage, V_{DS}, to protect the GaN FET from potential damage in the desaturation region. As illustrated in the timing diagram of Figure 16, when the V_{DS} exceeds the DESAT protection threshold (5.9V typical), the GaN FET is turned off. The GaN FET will be turned on again at the next rising edge of G signal. The blanking time of 600ns (typical) is added to prevent false triggering during the GaN FET turn-on.

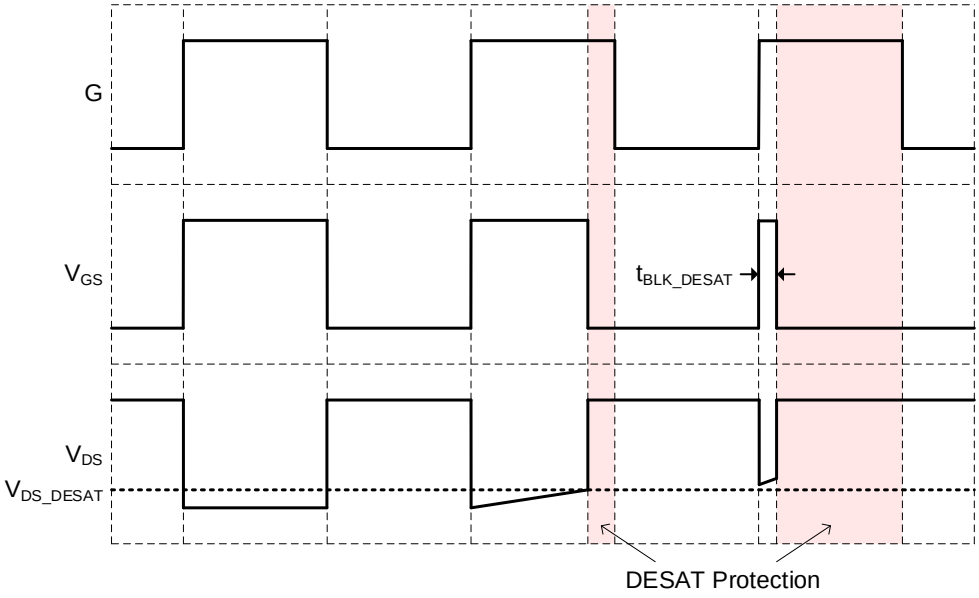
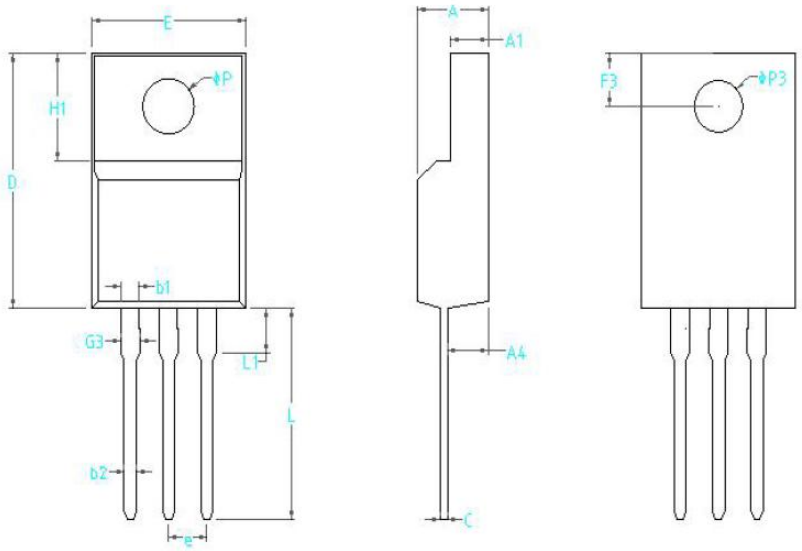
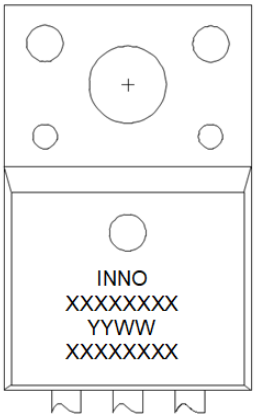


Figure 16. Timing Diagram of DESAT Protection

16. Package Information

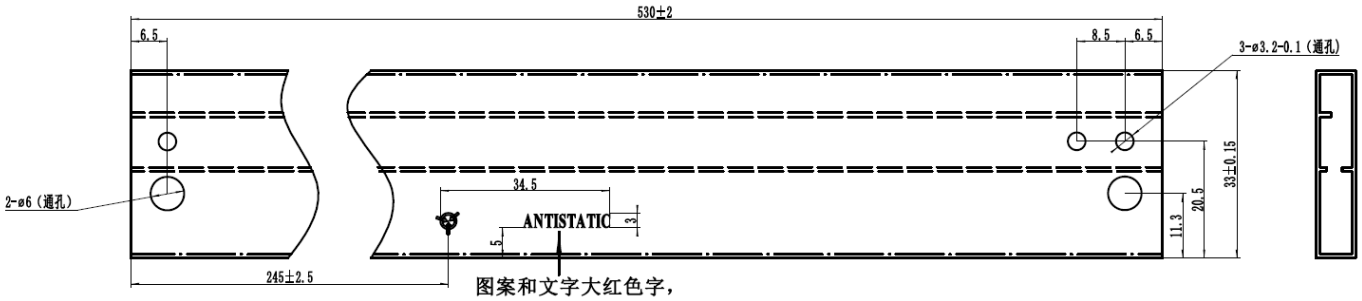


symbol	mm		
	min	nom	max
E	9.96	10.16	10.36
A	4.5	4.7	4.9
A1	2.34	2.54	2.74
A4	2.56	2.76	2.96
C	0.4	0.5	0.6
D	15.57	15.87	16.17
H1	6.5	6.8	7.1
e	2.34	2.54	2.74
L	12.73	13.03	13.33
L1	2.75	2.85	3.05
ΦP	3.2	3.4	3.6
ΦP3	2.98	3.18	3.38
F3	3.15	3.3	3.45
G3	1.12	1.27	1.42
b1	1.1	1.2	1.3
b2	0.7	0.8	0.9



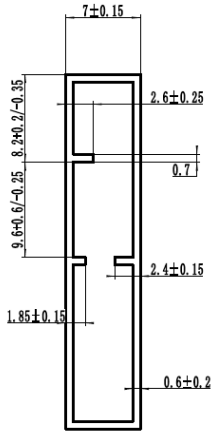
Row	Description	Example
Row1	Company Name	INNO
Row2	Product Code (In short)	XXXXXXXX
Row3	Date Code	YYWW
Row4	ASSY Lot No.	XXXXXXXX

17. Tube Information



图案和文字大红色字，
线宽0.5mm，实心印刷

相关要求
1、料管表面光洁透明、无污点、无缺角、无擦伤、无明显毛边现象；
2、干燥无水渍、油渍，无弯曲现象；
3、料管表面阻抗要求：1*10 e 6 Ω/Δ ~ 1*10 e 10 Ω/Δ；
4、未标注公差±0.25mm；
5、包装管互相摩擦电压＜100V；
6、符合RoHS要求；



18. Order Information

Ordering Code	Package	Product Code	Packing (Tube)
ISG6133TJ	TO220F	6133TJ	50PCS/Tube

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